NOT RECOMMENDED FOR NEW DESIGNS

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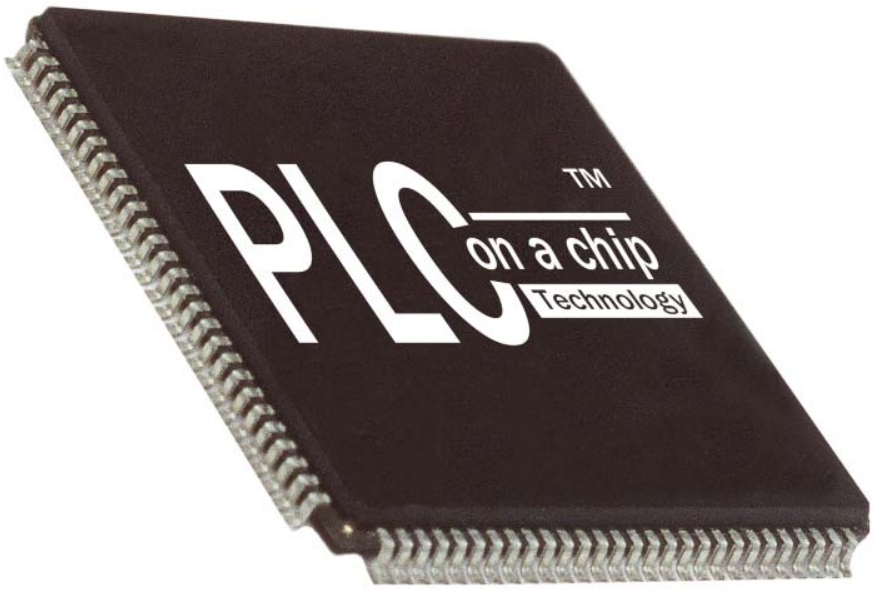

Patent 7,299,099

TECHNICAL DATA SHEET

Technical Data for *PLC on a Chip* Integrated Circuit Hardware Models

PLCHIP-M2-12800
PLCHIP-M2-25600
PLCHIP-M2-25620
PLCHIP-M2-25621
PLCHIP-M2-25622
PLCHIP-M2-25630
PLCHIP-M2-25631
PLCHIP-M2-25632
PLCHIP-M2-51230

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SECTION 1
OVERVIEW

Table of Contents

Revision History

Revision	Release Date	Description of Changes
Rev. A	06/08/2004	Initial Release of Data Sheet.
Rev. B		1. Corrected Errors. 2. Reorganized Datasheet & Separated Circuit Designs into separate document.
Rev. C		1. Corrected Errors.
Rev. D	8/10/2005	1. Updated Pin Descriptions and Alphabetized the Pin List. 2. Updated Specifications
Rev. E	3/15/2006	1. Corrected Errors 2. Updated Chip Part Numbers and Specifications for new chips per ECN 1466.
Rev. F	6/6/2007	1. Added I/O Pin Electrical Characteristics
Rev. G	12/13/2007	1. Added Patent Information 2. Removed PWM from PLCHIP-M2-12800. 3. Colorized Power Loss Pin for Emphasis

IMPORTANT NOTICE

Divelbiss reserves the right to discontinue or make changes to it's products without notice. Customers assume the responsibility for the appropriate application of Divelbiss components. It is the customer's responsibility to ensure that adequate design and operating safeguards are addressed to eliminate any hazards inherent to their application.

Definitions

EEPROM	Electrically erasable-programmable read only memory
FLASH	A type of non-volatile memory
HDIO	Divelbiss high density input output bus
LQFP	Leaded quad flat package
SRAM	Static random access memory
TTL	Transistor-transistor logic
SSI	Synchronous Serial Interface
CAN	Controller Area Network

About this Data Sheet

This data sheet is provided to provide technical information on the PLC on a Chip integrated circuit. This document provides the information listed in the Table of Contents.

For circuit design information, including recommendations on PLC on a Chip circuitry considerations including layout, PCB design, recommended required circuitry and peripheral circuitry including I/O, please refer the the **PLC on a Chip Circuit Design Guidelines** document.

For specific information regarding configuring a PLC on a Chip IC for use in EZ LADDER, refer to the **PLC on a Chip EZ LADDER Configuration** document.

CAUTION!!!

When handling the PLC on a Chip, please follow component ESD handling procedures to prevent the PLC on a Chip being damaged by electro-static discharge.

PLCHIP-M2-12800

Memory		
	FLASH	128KB
	EEPROM	2KB
	SRAM	8KB
Power supply	5VDC	
Package	112LQFP	
Temperature	-40°C - +85°C	
Communications	Asynchronous Serial:	1 - TTL Programming port
	Baud Rate:	57600 bps
Input / Output	Analog Input	8 channels 0-5VDC 10bit
	Digital Input	Up to 33 0-5 VDC inputs
	Digital Output	Up to 33 0-5 VDC outputs
	Divelbiss HDIO bus	128 inputs on HDIO modules 24VAC 115VAC 10-24VDC 128 outputs on HDIO modules 10-24VDC @ 1A 24-115VAC @ 1A Relay @ 5A Form C Relay @ 10A
Programming	Programs using Divelbiss EZ Ladder, a ladder diagram and function block development platform.	

PLCHIP-M2-25600

Memory		
	FLASH 256KB EEPROM 4KB SRAM 12KB	
Power supply	5VDC	
Package	112LQFP	
Temperature	-40°C - +85°C	
Communications	Asynchronous Serial: Baud Rate:	1 - TTL Programming port, 1 - TTL Multipurpose port Programming Port - 57600 bps TTL Multipurpose Port - 9600-57600 bps (115200 bps Modbus slave)
	Synchronous Serial:	SPI compatible, 2 - TTL level
Input / Output	Analog Input	8 channels 0-5VDC 10bit
	PWM Output	Up to 8 channels 8-bit or Up to 4 channels 16-bit
	Digital Input	Up to 33 0-5 VDC inputs
	Digital Output	Up to 33 0-5 VDC outputs
	Divelbiss HDIO bus	128 inputs on HDIO modules 24VAC 115VAC 10-24VDC 128 outputs on HDIO modules 10-24VDC @ 1A 24-115VAC @ 1A Relay @ 5A Form C Relay @ 10A
Programming	Programs using Divelbiss EZ Ladder, a ladder diagram and function block development platform.	

PLCHIP-M2-2562X

Memory

FLASH	256KB
EEPROM	4KB
SRAM	12KB

Power supply 5VDC

Package 112LQFP

Temperature
-40°C - +85°C (-0 option)
-40°C - +105°C (-1 option)
-40°C - +125°C (-2 option)

Communications

Asynchronous Serial: Baud Rate:	1 - TTL Programming port, 1 - TTL Multipurpose port Programming Port - 57600 bps TTL Multipurpose Port - 9600-57600 bps (115200 bps Modbus slave)
Synchronous Serial:	SPI compatible, 2 - TTL level
CAN	Up to 3 TTL level CAN ports

Input / Output

Analog Input	8 channels 0-5VDC 10bit
PWM Output	Up to 8 channels 8-bit or Up to 4 channels 16-bit
Digital Input	Up to 33 0-5 VDC inputs
Digital Output	Up to 33 0-5 VDC outputs
Divelbiss HDIO bus	128 inputs on HDIO modules 24VAC 115VAC 10-24VDC 128 outputs on HDIO modules 10-24VDC @ 1A 24-115VAC @ 1A Relay @ 5A Form C Relay @ 10A

Programming Programs using Divelbiss EZ Ladder, a ladder diagram and function block development platform.

PLCHIP-M2-2563X

(This part not recommended for new designs, use PLCHIP-M2-2562X instead)

Memory

FLASH	256KB
EEPROM	4KB
SRAM	12KB

Power supply 5VDC

Package 112LQFP

Temperature

-40°C - +85°C (-0 option)
-40°C - +105°C (-1 option)
-40°C - +125°C (-2 option)

Communications

Asynchronous Serial: Baud Rate:	1 - TTL Programming port, 1 - TTL Multipurpose port Programming Port - 57600 bps TTL Multipurpose Port - 9600-57600 bps (115200 bps Modbus slave)
Synchronous Serial:	SPI compatible, 2 - TTL level
CAN	Up to 5 TTL level CAN ports

Input / Output

Analog Input	8 channels 0-5VDC 10bit
PWM Output	Up to 8 channels 8-bit or Up to 4 channels 16-bit
Digital Input	Up to 33 0-5 VDC inputs
Digital Output	Up to 33 0-5 VDC outputs
Divelbiss HDIO bus	128 inputs on HDIO modules 24VAC 115VAC 10-24VDC 128 outputs on HDIO modules 10-24VDC @ 1A 24-115VAC @ 1A Relay @ 5A Form C Relay @ 10A

Programming Programs using Divelbiss EZ Ladder, a ladder diagram and function block development platform.

PLCHIP-M2-5123X

Memory		
	FLASH	512KB
	EEPROM	4KB
	SRAM	14KB
Power supply	5VDC	
Package	112LQFP	
Temperature	-40°C - +85°C (-0 option)	
Communications	Asynchronous Serial:	1 - TTL Programming port, 1 - TTL Multipurpose port
	Baud Rate:	Programming Port - 57600 bps TTL Multipurpose Port - 9600-57600 bps (115200 bps Modbus slave)
	Synchronous Serial:	SPI compatible, 2 - TTL level
	CAN	Up to 5 TTL level CAN ports
Input / Output	Analog Input	8 channels 0-5VDC 10bit
	PWM Output	Up to 8 channels 8-bit or Up to 4 channels 16-bit
	Digital Input	Up to 33 0-5 VDC inputs
	Digital Output	Up to 33 0-5 VDC outputs
	Divelbiss HDIO bus	128 inputs on HDIO modules 24VAC 115VAC 10-24VDC 128 outputs on HDIO modules 10-24VDC @ 1A 24-115VAC @ 1A Relay @ 5A Form C Relay @ 10A
Programming	Programs using Divelbiss EZ Ladder, a ladder diagram and function block development platform.	

SECTION 2
SIGNAL DESCRIPTIONS

Pin Function Summary

Pin Number	Primary Function	Alternate Function	Description	EZ Ladder I/O Reference
1	GPO12	PWM3 [2]	ACTIVE HIGH DIGITAL OUTPUT / PULSE WIDTH MODULATION OUTPUT	GPO12
2	GPO13	PWM2 [2]	ACTIVE HIGH DIGITAL OUTPUT / PULSE WIDTH MODULATION OUTPUT	GPO13
3	GPO14	PWM1 [2]	ACTIVE HIGH DIGITAL OUTPUT / PULSE WIDTH MODULATION OUTPUT	GPO14
4	GPO15	PWM0 [2]	ACTIVE HIGH DIGITAL OUTPUT / PULSE WIDTH MODULATION OUTPUT	GPO15
5	/GPI0	-----	ACTIVE LOW DIGITAL INPUT	GPI0
6	/GPI9	-----	ACTIVE LOW DIGITAL INPUT	GPI9
7	/GPI10	-----	ACTIVE LOW DIGITAL INPUT	GPI10
8	/GPI11	-----	ACTIVE LOW DIGITAL INPUT	GPI11
9	CNT_A	-----	COUNTER INPUT CHANNEL A	-----
10	N/C	-----	NOT CONNECTED	-----
11	N/C	-----	NOT CONNECTED	-----
12	N/C	-----	NOT CONNECTED	-----
13	INT_SUP0	-----	INTERNAL VOLTAGE SUPPLY, CONNECT ONLY TO SPECIFIED COMPONENTS	-----
14	GND (VSS)	-----	CONNECT TO DIGITAL GROUND	-----
15	N/C	-----	NOT CONNECTED	-----
16	N/C	-----	NOT CONNECTED	-----
17	N/C	-----	NOT CONNECTED	-----
18	CNT_B	-----	COUNTER INPUT CHANNEL B	-----
19	/GPI25	-----	ACTIVE LOW DIGITAL INPUT	GPI25
20	WD_OUT	-----	WATCHDOG OUTPUT	
21	/GPI16	-----	ACTIVE LOW DIGITAL INPUT	GPI16
22	/GPI15	-----	ACTIVE LOW DIGITAL INPUT	GPI15
23	Vsense1	-----	USED FOR INTERNAL PLC ON A CHIP CIRCUITRY. REQUIRES PULL-UP RESISTOR (1K)	-----
24	GPO6	-----	ACTIVE HIGH DIGITAL OUTPUT	GPO6
25	GPO3	-----	ACTIVE HIGH DIGITAL OUTPUT	GPO3
26	GPO2	-----	ACTIVE HIGH DIGITAL OUTPUT	GPO2
27	GPO32	HDIO_BBIN	ACTIVE HIGH DIGITAL OUTPUT / DIVELBISS HIGH DENSITY I/O EXPANSION BUS SIGNAL	GPO32

[1] This CAN port is only available on the PLCHIP-M2-51230 & PLCHIP-M2-2563X
[2] Not Available on the the PLCHIP-M2-12800

Pin Function Summary (Con't)

Pin Number	Primary Function	Alternate Function	Description	EZ Ladder I/O Reference
28	GPO16	HDIO_BBOUT	ACTIVE HIGH DIGITAL OUTPUT / DIVELBISS HIGH DENSITY I/O EXPANSION BUS SIGNAL	GPO16
29	GPO31	HDIO_BBRESET	ACTIVE HIGH DIGITAL OUTPUT / DIVELBISS HIGH DENSITY I/O EXPANSION BUS SIGNAL	GPO31
30	GPO18	HDIO_BBCLK	ACTIVE HIGH DIGITAL OUTPUT / DIVELBISS HIGH DENSITY I/O EXPANSION BUS SIGNAL	GPO18
31	GPO17	HDIO_BBWR	ACTIVE HIGH DIGITAL OUTPUT / DIVELBISS HIGH DENSITY I/O EXPANSION BUS SIGNAL	GPO17
32	GPO0	-----	ACTIVE HIGH DIGITAL OUTPUT	GPO0
33	GPO1	-----	ACTIVE HIGH DIGITAL OUTPUT	GPO1
34	GPO5	-----	ACTIVE HIGH DIGITAL OUTPUT	GPO5
35	GPO4	-----	ACTIVE HIGH DIGITAL OUTPUT	GPO4
36	N/C	-----	NOT CONNECTED	-----
37	GND (VSS)	-----	CONNECT TO DIGITAL GROUND	-----
38	GND (VSS)	-----	CONNECT TO DIGITAL GROUND	-----
39	/GPI14	-----	ACTIVE LOW DIGITAL INPUT	GPI14
40	GND (VSS)	-----	CONNECT TO DIGITAL GROUND	-----
41	+5VDC (VDD)	-----	CONNECT TO +5V SUPPLY	-----
42	/RESET	-----	BI-DIRECTIONAL RESET - ACTIVE LOW	-----
43	PVD	-----	USED WITH INTERNAL PLC ON A CHIP CIRCUITRY	-----
44	PSIG	-----	USED WITH INTERNAL PLC ON A CHIP CIRCUITRY	-----
45	PVS	-----	USED WITH INTERNAL PLC ON A CHIP CIRCUITRY	-----
46	EXTAL	-----	USED FOR OSCILLATOR	-----
47	XTAL	-----	USED FOR OSCILLATOR	-----
48	GND (VSS)	-----	CONNECT TO DIGITAL GROUND	-----
49	RTC_CE	-----	CHIP ENABLE SIGNAL FOR THE REAL TIME CLOCK	-----
50	SCK1	-----	SPI PORT 1 CLOCK - OUTPUT SIGNAL	-----
51	MOSI1	-----	SPI PORT 1 MASTER OUT SLAVE IN - OUTPUT SIGNAL	-----
52	MISO1	-----	SPI PORT 1 MASTER IN SLAVE OUT - INPUT SIGNAL	-----
53	/GPI13	-----	ACTIVE LOW DIGITAL INPUT	GPI13
54	/GPI12	-----	ACTIVE LOW DIGITAL INPUT	GPI12

[1] This CAN port is only available on the PLCHIP-M2-51230 & PLCHIP-M2-2563X
[2] Not Available on the the PLCHIP-M2-12800

Pin Function Summary (Con't)

Pin Number	Primary Function	Alternate Function	Description	EZ Ladder I/O Reference
55	/GPI33	-----	ACTIVE LOW DIGITAL INPUT	GPI33
56	/LOW_VOLTAGE	-----	ACTIVE LOW LOW VOLTAGE SENSE INPUT	None
57	GPO26	HDIO_ADDR_0	ACTIVE HIGH DIGITAL OUTPUT / DIVELBISS HIGH DENSITY I/O EXPANSION BUS SIGNAL	GPO26
58	GPO25	HDIO_ADDR_1	ACTIVE HIGH DIGITAL OUTPUT / DIVELBISS HIGH DENSITY I/O EXPANSION BUS SIGNAL	GPO25
59	GPO24	HDIO_ADDR_2	ACTIVE HIGH DIGITAL OUTPUT / DIVELBISS HIGH DENSITY I/O EXPANSION BUS SIGNAL	GPO24
60	GPO23	HDIO_ADDR_3	ACTIVE HIGH DIGITAL OUTPUT / DIVELBISS HIGH DENSITY I/O EXPANSION BUS SIGNAL	GPO23
61	GPO22	HDIO_ADDR_4	ACTIVE HIGH DIGITAL OUTPUT / DIVELBISS HIGH DENSITY I/O EXPANSION BUS SIGNAL	GPO22
62	GPO21	HDIO_ADDR_5	ACTIVE HIGH DIGITAL OUTPUT / DIVELBISS HIGH DENSITY I/O EXPANSION BUS SIGNAL	GPO21
63	GPO20	HDIO_ADDR_6	ACTIVE HIGH DIGITAL OUTPUT / DIVELBISS HIGH DENSITY I/O EXPANSION BUS SIGNAL	GPO20
64	GPO19	HDIO_ADDR_7	ACTIVE HIGH DIGITAL OUTPUT / DIVELBISS HIGH DENSITY I/O EXPANSION BUS SIGNAL	GPO19
65	INT_SUP1	-----	INTERNAL VOLTAGE SUPPLY, CONNECT ONLY TO SPECIFIED COMPONENTS	-----
66	GND (VSS)	-----	CONNECT TO DIGITAL GROUND	-----
67	/GPI17	AN0	ACTIVE LOW DIGITAL INPUT / ANALOG INPUT	/GPI17 / AN0
68	/GPI1	-----	ACTIVE LOW DIGITAL INPUT	GPI1
69	/GPI18	AN1	ACTIVE LOW DIGITAL INPUT / ANALOG INPUT	/GPI18 / AN1
70	/GPI2	-----	ACTIVE LOW DIGITAL INPUT	GPI2
71	/GPI19	AN2	ACTIVE LOW DIGITAL INPUT / ANALOG INPUT	/GPI19 / AN2
72	/GPI3	-----	ACTIVE LOW DIGITAL INPUT	GPI3
73	/GPI20	AN3	ACTIVE LOW DIGITAL INPUT / ANALOG INPUT	/GPI20 / AN3
74	/GPI4	-----	ACTIVE LOW DIGITAL INPUT	GPI4
75	/GPI21	AN4	ACTIVE LOW DIGITAL INPUT / ANALOG INPUT	/GPI21 / AN4
76	/GPI5	-----	ACTIVE LOW DIGITAL INPUT	GPI5

[1] This CAN port is only available on the PLCHIP-M2-51230 & PLCHIP-M2-2563X
[2] Not Available on the the PLCHIP-M2-12800

Pin Function Summary (Con't)

Pin Number	Primary Function	Alternate Function	Description	EZ Ladder I/O Reference
77	/GPI22	AN5	ACTIVE LOW DIGITAL INPUT / ANALOG INPUT	/GPI22 / AN5
78	/GPI6	-----	ACTIVE LOW DIGITAL INPUT	GPI6
79	/GPI23	AN6	ACTIVE LOW DIGITAL INPUT / ANALOG INPUT	/GPI23 / AN6
80	/GPI7	-----	ACTIVE LOW DIGITAL INPUT	GPI7
81	/GPI24	AN7	ACTIVE LOW DIGITAL INPUT / ANALOG INPUT	/GPI24 / AN7
82	/GPI8	-----	ACTIVE LOW DIGITAL INPUT	GPI8
83	+5VDC (VDD)	-----	CONNECT TO +5V SUPPLY	-----
84	+5VDC (VDD)	-----	CONNECT TO +5V SUPPLY	-----
85	GND (VSS)	-----	CONNECT TO DIGITAL GROUND	-----
86	GND (VSS)	-----	CONNECT TO DIGITAL GROUND	-----
87	/CTS1[2]	CANTX3 [1,2]	CLEAR TO SEND / CAN3 TRANSMIT SIGNAL	-----
88	/RTS1[2]	CANRX3 [1,2]	READY TO SEND / CAN 3 RECEIVE SIGNAL	-----
89	RXD0	-----	COM0 RECEIVE SIGNAL	-----
90	TXD0	-----	COM0 TRANSMIT SIGNAL	-----
91	RXD1[2]	-----	COM1 RECEIVE SIGNAL	-----
92	TXD1[2]	-----	COM1 TRANSMIT SIGNAL	-----
93	/GPI32	MISO0 [2]	ACTIVE LOW DIGITAL INPUT / SPI0 MASTER IN SLAVE OUT SIGNAL (CONSULT FACTORY)	GPI32
94	/GPI31	MOSI0 [2]	ACTIVE LOW DIGITAL INPUT / SPI0 MASTER OUT SLAVE IN SIGNAL (CONSULT FACTORY)	GPI31
95	/GPI30	SCK0 [2]	ACTIVE LOW DIGITAL INPUT / SPI0 CLOCK SIGNAL (CONSULT FACTORY)	GPI30
96	/GPI29	/SS0 [2]	ACTIVE LOW DIGITAL INPUT / SPI0 SLAVE SELECT SIGNAL (CONSULT FACTORY)	GPI29
97	VSENSE2	-----	USED FOR INTERNAL PLC ON A CHIP CIRCUITRY. REQUIRES PULL-UP RESISTOR (1K)	-----
98	/RTS0	CANTX4 [2]	COM0 ACTIVE LOW READY TO SEND SIGNAL / CAN4 TRANSMIT SIGNAL	-----
99	/CTS0	CANRX4 [2]	COM0 ACTIVE LOW CLEAR TO SEND SIGNAL / CAN4 RECIVE SIGNAL	-----
100	GPO7	CANTX2 [1,2]	ACTIVE HIGH DIGITAL OUTPUT / CAN2 TRANSMIT SIGNAL	GPO7

[1] This CAN port is only available on the PLCHIP-M2-51230 & PLCHIP-M2-2563X
[2] Not Available on the the PLCHIP-M2-12800

Pin Function Summary (Con't)

Pin Number	Primary Function	Alternate Function	Description	EZ Ladder I/O Reference
101	/GPI27	CANRX2 [1, 2]	ACTIVE LOW DIGITAL INPUT / CAN2 RECEIVE SIGNAL	GPI27
102	GPO27	CANTX1 [2]	ACTIVE HIGH DIGITAL OUTPUT / CAN1 TRANSMIT SIGNAL	GPO27
103	GPO30	CANRX1 [2]	ACTIVE HIGH DIGITAL OUTPUT / CAN1 RECEIVE SIGNAL	GPO30
104	GPO28	CANTX0 [2]	ACTIVE HIGH DIGITAL OUTPUT / CAN0 TRANSMIT SIGNAL	GPO28
105	GPO29	CANRX0 [2]	ACTIVE HIGH DIGITAL OUTPUT / CAN0 RECEIVE SIGNAL	GPO29
106	GND (VSS)	-----	CONNECT TO DIGITAL GROUND	-----
107	+5VDC (VDD)	-----	CONNECT TO +5V SUPPLY	-----
108	/GPI26	-----	ACTIVE LOW DIGITAL INPUT	GPI26
109	GPO8	PWM7 [2]	ACTIVE HIGH DIGITAL OUTPUT / PULSE WIDTH MODULATION OUTPUT	GPO8
110	GPO9	PWM6 [2]	ACTIVE HIGH DIGITAL OUTPUT / PULSE WIDTH MODULATION OUTPUT	GPO9
111	GPO10	PWM5 [2]	ACTIVE HIGH DIGITAL OUTPUT / PULSE WIDTH MODULATION OUTPUT	GPO10
112	GPO11	PWM4 [2]	ACTIVE HIGH DIGITAL OUTPUT / PULSE WIDTH MODULATION OUTPUT	GPO11

[1] This CAN port is only available on the PLCHIP-M2-51230 & PLCHIP-M2-2563X
[2] Not Available on the the PLCHIP-M2-12800

Refer to the "Circuit Design Guidelines" document ID DS-0470104-3-*X*.pdf. This document provides details on PIN Terminations and Interface Circuit Examples.

Electrical Characteristics Per I/O Pin

Pin Number	Primary Function	Alternate Function	Electrical Characteristic
1	GPO12	PWM3 [2]	High Impedance during reset. A pull-up or pull-down is recommended.
2	GPO13	PWM2 [2]	High Impedance during reset. A pull-up or pull-down is recommended.
3	GPO14	PWM1 [2]	High Impedance during reset. A pull-up or pull-down is recommended.
4	GPO15	PWM0 [2]	High Impedance during reset. A pull-up or pull-down is recommended.
5	/GPI0	-----	Internally pulled-up, 14-25 Kohm
6	/GPI9	-----	Internally pulled-up, 14-25 Kohm
7	/GPI10	-----	Internally pulled-up, 14-25 Kohm
8	/GPI11	-----	Internally pulled-up, 14-25 Kohm
9	CNT_A	-----	High Impedance during reset. A pull-up or pull-down is recommended.
18	CNT_B	-----	High Impedance during reset. A pull-up or pull-down is recommended.
19	/GPI25	-----	Internally pulled-up, 14-25 Kohm
20	WD_OUT	-----	Internally pulled-up, 14-25 Kohm
21	/GPI16	-----	High Impedance during reset. A pull-up or pull-down is recommended.
22	/GPI15	-----	High Impedance during reset. A pull-up or pull-down is recommended.
24	GPO6	-----	Internally pulled-up, 14-25 Kohm
25	GPO3	-----	Internally pulled-up, 14-25 Kohm
26	GPO2	-----	Internally pulled-up, 14-25 Kohm
27	GPO32	HDIO_BBIN	Internally pulled-up, 14-25 Kohm
28	GPO16	HDIO_BBOUT	Internally pulled-up, 14-25 Kohm
29	GPO31	HDIO_BBRESET	Internally pulled-up, 14-25 Kohm
30	GPO18	HDIO_BBCLK	Internally pulled-up, 14-25 Kohm
31	GPO17	HDIO_BBWR	Internally pulled-up, 14-25 Kohm
32	GPO0	-----	High Impedance during reset. A pull-up or pull-down is recommended.
33	GPO1	-----	High Impedance during reset. A pull-up or pull-down is recommended.
34	GPO5	-----	High Impedance during reset. A pull-up or pull-down is recommended.
35	GPO4	-----	High Impedance during reset. A pull-up or pull-down is recommended.
39	/GPI14	-----	Internally pulled-up, 14-25 Kohm

Electrical Characteristics Per I/O Pin (Cont'd)

Pin Number	Primary Function	Alternate Function	Electrical Characteristic
51	MOSI1	-----	High Impedance during reset. A pull-up or pull-down is recommended.
52	MISO1	-----	High Impedance during reset. A pull-up or pull-down is recommended.
53	/GPI13	-----	Internally pulled-up, 14-25 Kohm
54	/GPI12	-----	Internally pulled-up, 14-25 Kohm
55	/GPI33	-----	Internally pulled-up, 14-25 Kohm
56	/LOW_VOLTAGE	-----	Internally pulled-up, 14-25 Kohm
57	GPO26	HDIO_ADDR_0	Internally pulled-up, 14-25 Kohm
58	GPO25	HDIO_ADDR_1	Internally pulled-up, 14-25 Kohm
59	GPO24	HDIO_ADDR_2	Internally pulled-up, 14-25 Kohm
60	GPO23	HDIO_ADDR_3	Internally pulled-up, 14-25 Kohm
61	GPO22	HDIO_ADDR_4	Internally pulled-up, 14-25 Kohm
62	GPO21	HDIO_ADDR_5	Internally pulled-up, 14-25 Kohm
63	GPO20	HDIO_ADDR_6	Internally pulled-up, 14-25 Kohm
64	GPO19	HDIO_ADDR_7	Internally pulled-up, 14-25 Kohm
67	/GPI17	AN0	Always High Impedance
68	/GPI1	-----	Always High Impedance
69	/GPI18	AN1	Always High Impedance
70	/GPI2	-----	Always High Impedance
71	/GPI19	AN2	Always High Impedance
72	/GPI3	-----	Always High Impedance
73	/GPI20	AN3	Always High Impedance
74	/GPI4	-----	Always High Impedance
75	/GPI21	AN4	Always High Impedance
76	/GPI5	-----	Always High Impedance
77	/GPI22	AN5	Always High Impedance
78	/GPI6	-----	Always High Impedance
79	/GPI23	AN6	Always High Impedance
80	/GPI7	-----	Always High Impedance
81	/GPI24	AN7	Always High Impedance
82	/GPI8	-----	Always High Impedance

Electrical Characteristics Per I/O Pin (Cont'd)

Pin Number	Primary Function	Alternate Function	Electrical Characteristic
93	/GPI32	MISO0 [2]	High Impedance during reset. A pull-up or pull-down is recommended.
94	/GPI31	MOSI0 [2]	High Impedance during reset. A pull-up or pull-down is recommended.
95	/GPI30	SCK0 [2]	High Impedance during reset. A pull-up or pull-down is recommended.
96	/GPI29	/SS0 [2]	High Impedance during reset. A pull-up or pull-down is recommended.
100	GPO7	CANTX2 [1, 2]	High Impedance during reset. A pull-up or pull-down is recommended.
101	/GPI27	CANRX2 [1, 2]	High Impedance during reset. A pull-up or pull-down is recommended.
102	GPO27	CANTX1 [2]	High Impedance during reset. A pull-up or pull-down is recommended.
103	GPO30	CANRX1 [2]	High Impedance during reset. A pull-up or pull-down is recommended.
104	GPO28	CANTX0 [2]	High Impedance during reset. A pull-up or pull-down is recommended./ CAN0 TRANSMIT SIGNAL
105	GPO29	CANRX0 [2]	High Impedance during reset. A pull-up or pull-down is recommended.
108	/GPI26	-----	Internally pulled-up, 14-25 Kohm
109	GPO8	PWM7 [2]	High Impedance during reset. A pull-up or pull-down is recommended.
110	GPO9	PWM6 [2]	High Impedance during reset. A pull-up or pull-down is recommended.
111	GPO10	PWM5 [2]	High Impedance during reset. A pull-up or pull-down is recommended.
112	GPO11	PWM4 [2]	High Impedance during reset. A pull-up or pull-down is recommended.

Detailed Signal Descriptions

+5VDC (VDD)

These pins are the main power supply pins for the PLC on a Chip. They must be supplied with +5VDC. Adequate noise decoupling is required.

CNT_A / CNT_B

These input pins are hardware counter inputs.
The counters have the following specifications:
32-bit resolution
Maximum input frequency = 1MHz

/CTS0/CANRX4

Active low Clear To Send input signal for COM0. Secondary functionality as a CAN receive signal for CAN4.

/CTS1 / CANTX3

Active low clear to send input signal for COM1. Secondary functionality is a CAN transmit signal for CAN3.

EXTAL, XTAL

Used for oscillator.

GND (VSS)

These pins are to be connected to the system digital ground.

/GPIx

These pins are dedicated active low digital inputs.

/GPI17 - /GPI24, AN*x*

These active low digital input pins are multiplexed as analog inputs. When the analog input configuration is selected, all 8 inputs (/GPI17 - /GPI24) are configured as analog inputs The PLC on a Chip analog inputs have the following characteristics:
10-bit resolution.
Sampled at beginning of ladder scan.
0-5VDC input range

/GPI27 / CANRX2

This active low digital input pin has a secondary functionality as the receive signal for CAN2.

/GPI29 / /SS0

Active low digital input with secondary functionality as SPI0 active low slave select signal. Consult factory for SPI0 usage.

/GPI30 / SCK0

Active low digital input with secondary functionality as a SPI0 clock signal. Consult factory for SPI0 usage.

/GPI31 / MOSI0

Active low digital input with secondary functionality as a SPI0 master out slave in signal. Consult factory for SPI0 usage.

/GPI32 / MISO0

Active low digital input with secondary functionality as a SPI0 master in slave out signal. Consult factory for SPI0 usage.

GPO*x* / PWM*x*

These pins are digital output pins which have a secondary functionality as a Pulse Width Modulation output.

GPO*x*

These pins are dedicated digital outputs.

GPO*x* / HDIO_ADDR*x*

These digital output pins have a secondary function as the address lines for the Divelbiss HDIO expansion bus.

Detailed Signal Descriptions (Con't)

GPO7 / CANTX2
This digital output pin has a secondary functionality as the transmit signal for CAN2.

GPO16 / HDIO_BBOUT
This digital output pin has a secondary function as the BBOUT output for the Divelbiss HDIO expansion bus.

GPO17 / HDIO_BBWR
This digital output pin has a secondary function as the BBWR output for the Divelbiss HDIO expansion bus.

GPO18 / HDIO_BBCLK
This digital output pin has a secondary function as the BBCLK output for the Divelbiss HDIO expansion bus.

GPO27 / CANTX1
This digital output pin has a secondary functionality as the transmit signal for CAN1.

GPO28 / CANTX0
This digital output pin has a secondary functionality as the transmit signal for CAN0.

GPO29 / CANRX0
This digital output pin has a secondary functionality as the receive signal for CAN0.

GPO30 / CANRX1
This digital output pin has a secondary functionality as the receive signal for CAN1.

GPO31 / HDIO_BBRESET
This digital output pin has a secondary function as the BBRESET output for the Divelbiss HDIO expansion bus.

GPO32 / HDIO_BBIN
This digital output pin has a secondary function as the BBIN input for the Divelbiss HDIO expansion bus.

INT_SUP0,INT_SUP1
These pins are used to provide capacitance de-coupling for power supply circuits internal to the PLC on a Chip. ***ONLY THE CAPACITORS AS SPECIFIED IN THE PLC on a Chip CIRCUIT DESIGN Guidelines DOCUMENT SHOULD BE TERMINATED TO THESE PINS!***

/LOW_VOLTAGE
This active low input is for sensing a low system voltage. This pin is required for Retentive Memory features. This pin must be connected to +5V if a Low Voltage circuit is NOT used. The power supply hold up time must be 10 msec minimum to allow for all chip housekeeping in the event of a power failure.

MISO1
SPI port 1 master in slave out signal. Note that the PLC on a Chip is a master device.

MOSI1
SPI port 1 master out slave in signal. Note that the PLC on a Chip is a master device.

N/C
No connection is to be made to this pin.

PVS, PVD, PSIG
Used with internal PLC on a Chip circuitry. Refer to the "Circuit Design Guidelines" document.

/RESET
This pin is an active-low bi-directional signal used to initialize the PLC on a Chip to a known start-up condition. It also acts as an output when an internal reset occurs.

RTC_CE
Chip enable output for use with real time clock.

RTS0/CANTX4
Active low Ready To Send output signal for COM0. Secondary functionality as a CAN transmit signal for CAN4.

Detailed Signal Descriptions (Con't)

/RTS1 / CANRX3

Active low ready to send output signal for COM1. Secondary functionality is a CAN receive signal for CAN3.

RXD0

Asynchronous serial receive input - COM0. Used for programming with EZLADDER.

RXD1

Asynchronous serial receive input - COM1. General purpose. Used with serial communications function blocks in EZLADDER.

SCK1

SPI port 1 serial clock signal.

TXD0

Asynchronous serial transmit output - COM0. Used for programming with EZLADDER.

TXD1

Asynchronous serial receive output - COM1. General purpose. Used with serial communications function blocks in EZLADDER.

VSENSE1, VSENSE2

These input pins are for an internal voltage reference on the PLC on a Chip. They must be pulled up to the system digital +5VDC supply with a 1K resistor.

WD_OUT

This pin provides an output which will toggle to indicate that the PLC on a Chip is operating properly.

SECTION 3
ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Absolute maximum ratings indicate limits beyond which damage to the device may occur. Functionality outside of these ratings is indeterminate and reliability may be affected.

Rating	Min	Max	Unit
All I/O[1], +5VDC power pins voltage limits	-0.3	6.0	VDC
EXTAL, XTAL inputs voltage limits	-0.3	3.0	VDC
PSIG voltage limits	-0.3	3.0	VDC
Storage Temperature	-65	155	°C
VSENSE_ voltage limits	-0.3	6.0	VDC
/RESET voltage limits	-0.3	6.0	VDC

NOTES: 1. Voltage applied to I/O pins must not exceed voltage applied to +5VDC power pins.

Normal Operating Conditions

Normal operating conditions are the conditions for which the device is intended to be functional.

Rating	Min	Typ	Max	Unit
All I/O, +5VDC power pins - supply voltage (VDD)	4.5	5	5.25	VDC
Oscillator frequency		12.0		MHz
Ambient Temperature	-40		+85	°C
INT_SUP_[1] pins - operating voltage	2.35	2.5	2.75	VDC
VSENSE_ - supply voltage	-4.5	5	5.25	VDC
/RESET - release level			2.0	VDC
/RESET - assert level	0.9			VDC
/RESET - Minimum input pulse width	1			µS
/RESET - Startup time from reset	20			µS
All Inputs - Input High Voltage	.65 * VDD		VDD + .3	VDC
All Inputs - Input Low Voltage	VSS - .3		.35 * VDD	VDC
All Inputs - Input leakage current	-2.5		2.5	µA
All outputs - Output High Voltage $_{VOHMIN}$	VDD - .8			VDC
All outputs - Output Low Voltage $_{VOLMAX}$			0.8	VDC
All outputs - output current limit $_{IOMAX}$	-1.0		1.0	mA
Quiescent Supply Current[2]		45		mA
NVM EEPROM write cycle reliability[3]		10,000		Cycles
NVM EEPROM Data Retention Lifetime[3]		5		Years
Oscillator startup time		8	100	mS
Thermal resistance[4] Θ_{JA}			54	°C/W
Operating Junction Temperature Range T_J	-40		100	°C

NOTES:
1. This voltage is generated internally in the PLC on a Chip device. Only the bypass capacitors specified in the circuit design section of this document should be terminated to these pins.
2. Quiescent supply current varies widely from application to application. Actual current drive per output point must be added to this figure to determine total device current consumption.
3. Over entire operating temperature range.
4. Double sided FR4 PCB

Power Dissipation and Thermal Characteristics

$T_J = T_A + (P_D * \Theta_{JA})$

$P_D = V_{supply} * I_{supply} + P_{IO}$

V_{supply} = Actual supply voltage to PLC on a Chip

I_{supply} = Actual supply current to PLC on a Chip

$P_{IO} = P_1 + P_2$ = Total power dissipation from output pins where:

$P_1 = \Sigma(V_{OL} * I_{SUNK})$ for all outputs driven low

$P_2 = \Sigma((V_{supply} - V_{OH})) * I_{SOURCE}$ for all outputs driven high

V_{OL} = Actual voltage measured on pin

V_{OH} = Actual voltage measured on pin

I_{SUNK} = Current sunk through pin

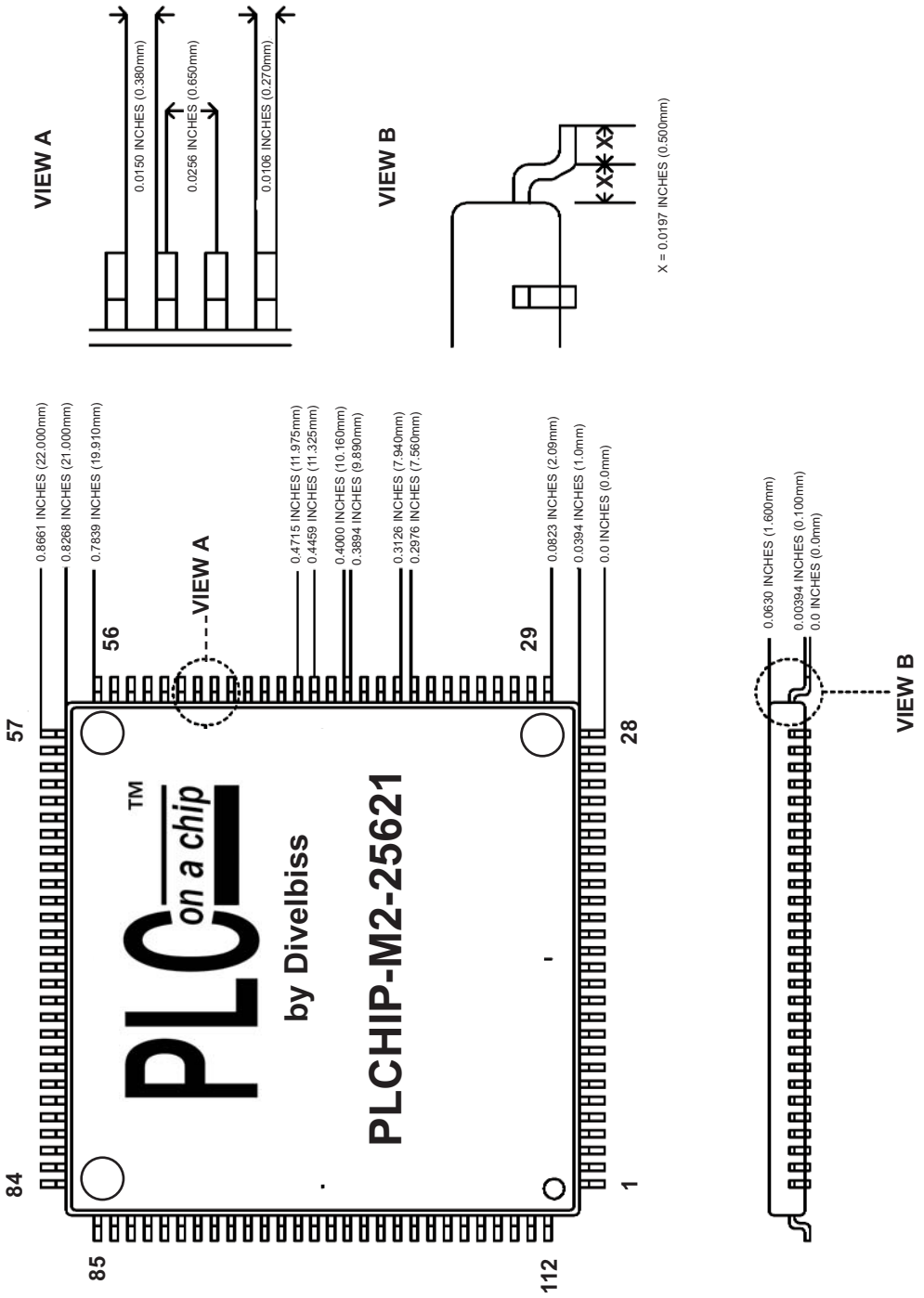
I_{SOURCE} = Current sourced from pin

I_{OL}, I_{OH} = Actual current sunk/sourced by pin

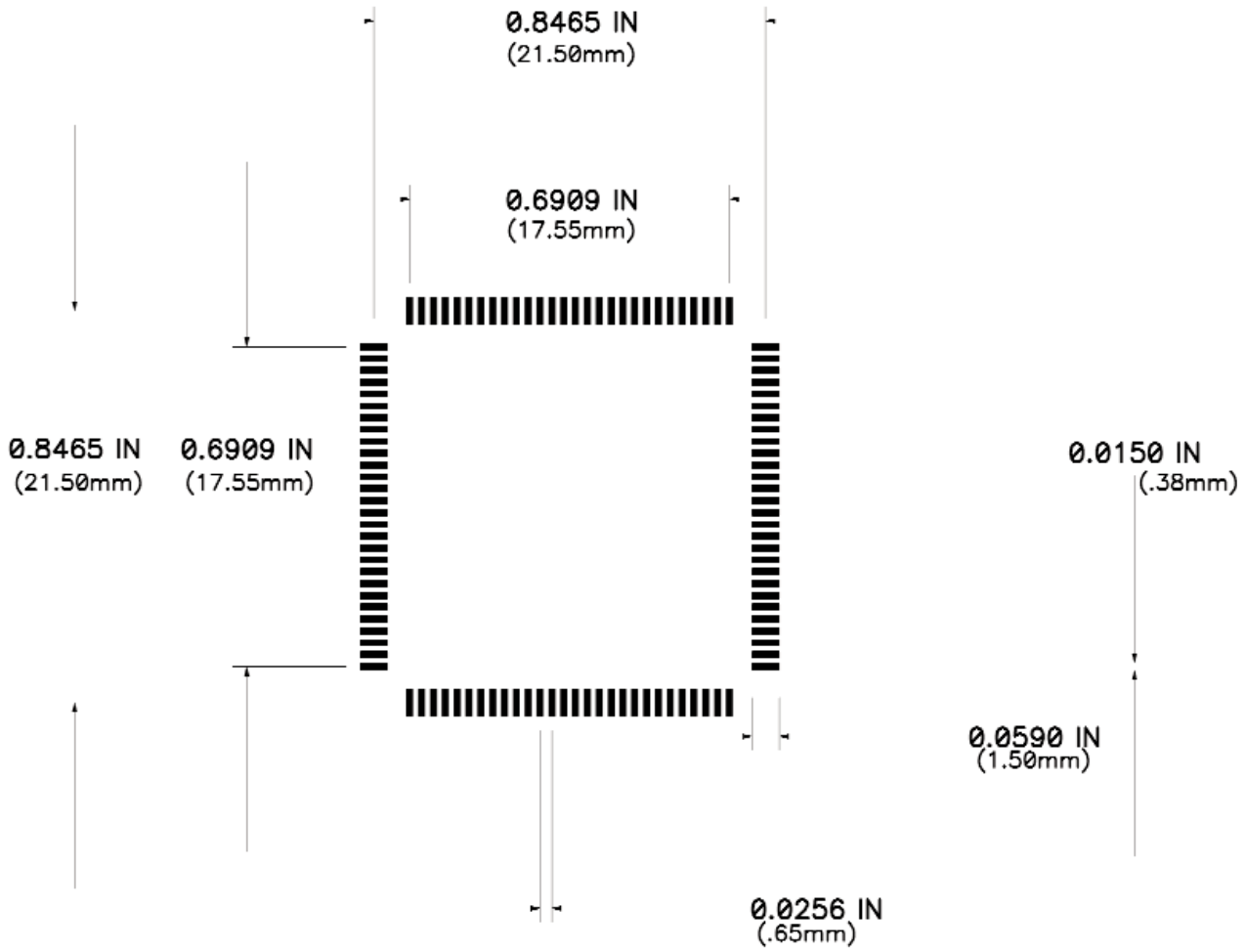
SECTION 4
PACKAGE INFORMATION

PLC on a Chip IC Dimensions

112-pin LQFP Package



SMT PCB Layout Recommendations



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